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10/603,252	06/25/2003	Thomas J. Heller JR.	POU920030046US1	3685

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EXAMINER	
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2187	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/603,252	HELLER, THOMAS J.	
	Examiner	Art Unit	
	Jared I. Rutz	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 October 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-30, as amended on 10/23/2007, are pending in the instant Office action. The instant Office action contains new grounds of rejection not necessitated by Amendment. Accordingly, this Office action is made non-final.

Specification

2. The Amendment to the specification submitted 10/23/2007 has been accepted by the Examiner.

3. The Amendment to the Abstract submitted 10/23/2007 has been accepted by the Examiner

4. The Drawings submitted 7/18/2007 have been accepted by the Examiner.

Claim Objections

5. **Claim 11** is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. Claim 11 recites the limitation "wherein if said another coherency region contains fewer hardware processing nodes than the original coherency region, the size of the coherency region has been effectively reduced." The Examiner respectfully notes that this limitation does not require that the "another coherency region" contains fewer processing nodes, and seems to merely be a definition of the size of a coherency region.

6. **Claims 24 and 27** are objected to because of the following informalities:

a. **Claim 24** recites the limitation "said supervision software". The Examiner respectfully submits that this should read "said supervisor software".

b. **Claim 27** recites the limitation "storage request which requests which hit". The Examiner respectfully submits that "request which" is unnecessary and unclear.

7. Appropriate correction is required.

Claim Rejections - 35 USC § 112

8. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. **Claims 1-30** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

10. The claims are generally narrative and indefinite, failing to conform with current U.S. practice. The structure of the phrases used, and the language used within the phrases fail to clearly set forth that which applicant seeks to protect. The wording of the claims tends more toward a discussion of the claimed invention rather than language particularly pointing out and distinctly claiming the metes and bounds of the claimed invention. Several examples of such language are presented infra.

11. **Claim 1** recites the limitation "said supervisor program" in line 14 (labeled as the second line 3 in the amendment submitted 10/23/2007). There is insufficient antecedent basis for this limitation in the claim.

12. **Claim 1** recites the limitation "the old nodes" in line 17 (labeled as the second line 6 in the amendment submitted 10/23/2007). There is insufficient antecedent basis for this limitation in the claim.

13. **Claim 1** recites the limitation "these old cache entries" in line 18 (labeled as the second line 7 in the amendment submitted 10/23/2007). There is insufficient antecedent basis for this limitation in the claim.

14. **Claim 1** recites the limitation "the new processing nodes" in lines 18-19 and 20-21 (labeled as the second lines 8-9 and 10-11 in the amendment submitted 10/23/2007). There is insufficient antecedent basis for this limitation in the claim.

15. **Claim 1** recites the limitation "the same main storage addresses" in lines 19-20 (labeled as the second lines 9-10 in the amendment submitted 10/23/2007). There is insufficient antecedent basis for this limitation in the claim. What are the main storage addresses the same as?

16. **Claim 1** recites the limitation "the old entries" in line 17 (labeled as line 11 in the amendment submitted 10/23/2007). There is insufficient antecedent basis for this limitation in the claim.

17. **Claim 1** recites the limitation "controlling software-initiated movement of software processes between said plurality of cache coherency regions by changing coherency mode bits without requiring a selective purging of cache contents in one or more of said

processing nodes". The requirements of this limitation are unclear, as there does not appear to be any requirement that the selective purging which is not required is not required in a processing node having any sort of connection to a software process being moved between cache coherency regions. For example, if a cache coherency region were defined that contained processors A and B, and a process executing on said cache coherency region was moved to a cache coherency region containing processors C and D, the cache belonging to processor E would not be required to be purged, as it does not contain any data relating to the moved process. However, it appears that the language of the claim would still allow the selective purging of the caches of processors A and B, which runs contrary to the summary of the invention provided at lines 5-18 of page 6 of the specification as originally filed. Accordingly, it is not clear what is not required to be purged.

18. **Claim 1** further recites the limitation "and when said supervisor program is moving a coherency region from one distinct set of processing nodes to another distinct set of processing nodes it is effectively leaving behind cache entries for the coherency region on the old nodes". It is unclear what it means to "effectively" leave behind cache entries. Additionally, the Examiner suspects that the "one distinct set of processing nodes" corresponds to "the old nodes" recited in line 17, and that "another distinct set of processing nodes" corresponds to " the new processing nodes" recited in lines 19-22, and suggests that Applicant amend claim 1 to make this clear if that is the intended meaning of said limitations.

19. **Claim 1** further recites the limitation "and that cache entries for the same main storage addresses will not be established in the new processing nodes until the old entries are invalidated". This claim seems to contradict the earlier limitation "without requiring a selective purging of cache contents in one or more of said processing nodes", as it seems to explicitly require selectively purging the old entries. The Examiner suspects that the purging is not required when the process is first moved, but is delayed until that address is accessed. The Examiner recommends amending the claim to clearly reflect the intended meaning.

20. **Claim 2** recites the limitation "said cache controller logic" in line 3. It appears from claim 1 that each processing node includes cache controller logic, so which cache controller logic is "said cache controller logic"? Is it the cache controller logic associated with the processor making the storage request, a cache controller logic associated with a processor receiving the incoming storage request or some other cache controller logic?

21. **Claim 2** further recites the limitation "including supervisor software which enables said cache controller logic in a processing node to be sure upon an incoming storage request". It is unclear what it means for supervisor software to enable cache controller logic to be sure of something. Does the limitation require that the supervisor software causes the cache controller logic to perform some sort of operation to make sure that no copy exists outside the requesting processor's current coherency region, or is the cache controller logic sure that no copy exists outside that processor's current coherency

region because the existence of the supervisor software prevents such a copy from existing.

22. **Claim 2** recites the limitation "said processing nodes" in line 10. There is insufficient antecedent basis for this limitation. Claim 1 recites a plurality of processing nodes in line 3, but also recites "one distinct set of processing nodes", "another distinct set of processing nodes", "the old nodes", and "the new processing nodes". Which processing nodes are being referred to in line 10 of claim 2?

23. **Claim 3** recites the limitation "for each process that has its own coherency region" in lines 3-4. Claim 2 lines 6-7 identifies coherency regions as being associated with processors, not processes. Accordingly, it is unclear if a process actually has its own coherency region, or if the coherency region is a property of the processor on which the process is running.

24. **Claim 4** recites the limitation "wherein supervisor software creates a table for each processing node in the system which has an entry for every Coherency Region ID that is currently allowed to be dispatched on said processing node". How many tables are created? Is one table created that is used by each processing node, or is a separate table created for each processing node? Does the table or the processing node have an entry?

25. **Claim 4** recites the limitation "said processing node" in line 5. There is insufficient antecedent basis for this limitation, as there a are a plurality of processing

nodes, and a plurality of groups of processing nodes recited in claims 1 and 2, from which claim 4 depends.

26. **Claim 5** recites the limitation "wherein said supervisor software creates a unique Coherency Region ID for each process that has its own coherency region and one or more coherency mode bits for each processor in the multiprocessor computer system, and said coherency mode bits and coherency region ID associated with a processor". It is unclear from this limitation if the coherency region IDs are associated with a process or with a processor.

27. **Claim 6** recites the limitation "wherein said supervisor software creates a unique Coherency Region ID for each process that has its own coherency region and one or more coherency mode bits for each processor in the multiprocessor system to to a node controller for a processor". The Examiner respectfully notes that the word "to" is repeated in lines 5 and 6 of claim 6. Additionally, it is unclear what it means to create a coherency region id and mode processor to a node controller. Additionally, it is unclear if the supervisor software creates a coherency region for each process and creates one or more coherency mode bits for each processor, or if it only creates a coherency region ID for a process, the process having its own coherency region and one or more coherency mode bits for each processor.

28. **Claim 7** recites the limitation "wherein said supervisor software creates a unique Coherency Region ID for each process that has its own coherency region and one or more coherency mode bits for each processor in the multi processor computer system". Again, it is unclear if the supervisor software creates a coherency region ID for each process and creates one or more coherency mode bits for each processor, or if the supervisor creates a unique coherency region ID for each process, each process having its own coherency region and one or more coherency mode bits for each processor.

29. **Claim 8** recites the limitation "wherein said supervisor software creates a unique Coherency Region ID for each process that has its own coherency region and one or more coherency mode bits for each processor in the multiprocessor computer system". Again, it is unclear if the supervisor software creates a coherency region ID for each process and creates one or more coherency mode bits for each processor, or if the supervisor creates a unique coherency region ID for each process, each process having its own coherency region and one or more coherency mode bits for each processor.

30. **Claim 9** recites the limitation "into another coherency region that has been created to cover the same address space as the first but which will include a new set of processing nodes". It is unclear what "the first" refers to.

31. **Claim 12** recites the limitation "wherein said multiprocessor computer system having a plurality of said processing nodes uses a table of active coherency region

information associated with each processing node" What is associated with each processing node, the table or the active coherency region information?

32. **Claim 13** recites the limitation "said tables" in line 3. There is insufficient antecedent basis for this limitation as there is only one table recited in claim 12.

33. Claim 13 recites the limitation "that processing node" in lines 5-6. There is insufficient antecedent basis for this limitation as claims 1 and 12 recite a plurality of processing nodes.

34. The term "large multiprocessor system" in **claim 21** is a relative term which renders the claim indefinite. The term "large" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

35. **Claim 22** recites the limitation "wherein said supervisor software creates a unique Coherency Region ID for each process that has its own coherency region and one or more coherency mode bits for each processor in the multiprocessor computer system". Again, it is unclear if the supervisor software creates a coherency region ID for each process and creates one or more coherency mode bits for each processor, or if the supervisor creates a unique coherency region ID for each process, each process

having its own coherency region and one or more coherency mode bits for each processor.

36. **Claim 25** recites the limitation "said coherency region ID" in line 2. There is insufficient antecedent basis for this limitation, as claims 1 and 2 do not recite a coherency region ID.

37. **Claim 28** recites the limitation "said supervisor software creates a table for each processing node in the multiprocessor computer system which has an entry for every Coherency Region ID that is currently allowed to be dispatched on said processing node". It is unclear if a table is only created for processing nodes that have an entry for every Coherency Region ID allowed to be dispatched, if a table is created for each processing node and the table has an entry for every Coherency Region ID that is allowed to be dispatched, or one table is created and that table is for all the processing nodes.

38. **Claim 29** recites the limitation "said coherency mode bits" in line 2. There is insufficient antecedent basis for this limitation.

39. **Claim 29** recites the limitation "coherency region ID associated with a processor". Claim 28 states that Coherency Region IDs are for processes, not processors.

40. **Claim 30** recites the limitation "enabling with supervisor software in the multiprocessor computer system's cache controller logic in a processing node to be sure that". It is unclear what it means for supervisor software to enable cache controller logic to be sure of something. Does the limitation require that the supervisor software causes the cache controller logic to perform some sort of operation to make sure that no copy exists outside the requesting processor's current coherency region, or is the cache controller logic sure that no copy exists outside that processor's current coherency region because the existence of the supervisor software prevents such a copy from existing.

41. **Claim 30** recites the limitation "said processing node" in line 5 (identified as line 6 in the amendment submitted 10/23/2007) and "said processing node's current coherency region" in line 7-8 (identified as lines 8-9 in the amendment submitted 10/23/2007. There is insufficient antecedent basis for these limitations, as a plurality of processing nodes have been recited and it is unclear which processing node would be "said processing node".

Allowable Subject Matter

42. Claims 1-30 appear to be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action. The Examiner notes that this statement is based on the Examiner's best interpretation of the claims in light of the specification and the issues presented supra with respect to 35 USC 112 second paragraph.

Response to Arguments

43. Applicant's arguments filed 10/23/2007 have been fully considered but they are not persuasive.

44. **First point of Argument**

45. In the second paragraph beginning on page 20 of the arguments submitted 10/23/2007, applicant argues:

c. "*In answer to the examiners question about the use of purge in the claim, which use was correct, and to answer the examiner's question it has been decided to combine the duplicate second claim 27 into claim 1, as that language is true for all claims and makes the use of purge in claim 1 clear to the person of ordinary skill in the art. Indeed purging occurs even though the moving of a coherency region from one set of processing nodes to another effectively leaves behind cache entries on the old nodes and that cache entries for the same main*

storage address will not be established in the new nodes until the old entries are invalidated."

46. The Examiner respectfully submits that Applicant's arguments do not sufficiently clarify the use of purge in claim 1. Although applicant states "indeed purging occurs", claim 1 explicitly states that the cache controller logic controls the movement of processes between cache coherency regions "without requiring a selective purging of cache contents in one or more of said processing nodes". The Examiner believes that that the issue is when the purging occurs, and encourages Applicant to make the timing clear if that is the case.

Conclusion

47. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

d. Glassen et al. (US 5,819,061) teaches a multiprocessor system with changeable partitions, but teaches that caches are purged when the partitions are reconfigured.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jared I. Rutz whose telephone number is (571) 272-5535. The examiner can normally be reached on M-F 8:00 AM - 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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